

# **MBI6812 Application Note**

#### **Foreword**

MBI6812 is an AC-DC constant current controller with primary side regulation (PSR), the imbedded active power factor correction (PFC) and quasi-resonant (QR) enhance the performance in LED lighting. MBI6812 also provides full protections including under voltage lock-out (UVLO), IC over voltage protection, MOSFET over current protection, LED open-circuit protection, LED short-circuit protection, current sense pin short to GND protection. The built-in Line compensation function corrects line regulation less than 1% without additional component.

## **Operation Principle**

Fig.1 is the typical application circuit of flyback converter based on MBI6812. When  $S_1$  is turned on, input voltage charges the magnetizing inductor, the secondary side is reversely-blocked by  $D_0$  and the load current is supplied by  $C_0$ . When  $S_1$  is turned off, the energy stored on the magnetizing inductor is discharged to the secondary side and therefore supplies the load current and recharges  $C_0$ .

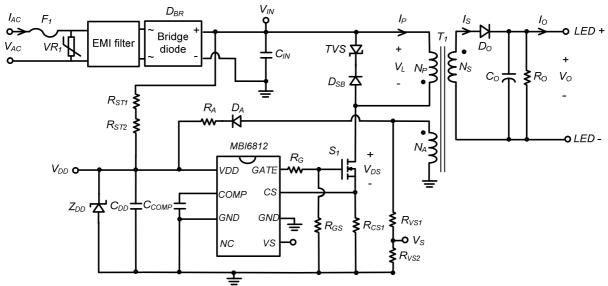


Fig.1 Typical application circuit of MBI6812



## **Primary Side Regulation**

Fig.2 shows the typical waveforms of DCM flyback converter, in which  $t_{on}$  is the conducting time of  $S_1$ ,  $t_{dsc}$  is the conducting time of  $D_0$ , and  $T_S$  is a single switching period. When the secondary side current  $I_S$  drops to zero,  $V_S$  will drop accordingly. Thus,  $t_{dsc}$  can be determined by detecting the onset of  $V_S$  falling edge.

The average output current can be derived by

$$I_{o} = \frac{1}{2} \cdot \frac{t_{dsc}}{T_{s}} \cdot I_{s, pk}$$

$$= \frac{1}{2} \cdot \frac{t_{dsc}}{T_{s}} \cdot \frac{N_{P}}{N_{S}} \cdot I_{p, pk}$$

$$= \frac{1}{2} \cdot \frac{t_{dsc}}{T_{s}} \cdot \frac{N_{P}}{N_{S}} \cdot \frac{V_{cs, pk}}{R_{cs}}$$

$$(2)$$

MBI6812 detects  $V_{cs,pk}$  and  $t_{dsc}$  through CS and VS pins respectively, so that the output current  $I_O$  can be derived and regulated.

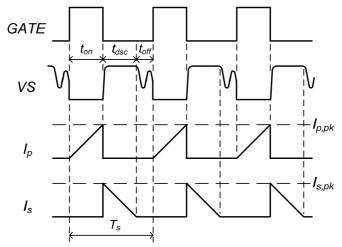


Fig.2 Typical waveform of DCM flyback



#### **Active Mode Power Factor Correction**

Theoretically, when the input main voltage and input current are in phase and proportional to each other, the power factor will be unity. In a flyback converter, this is equivalent to the proportionality between the voltage across the magnetizing inductor,  $V_{LM}$ , and the average current of the primary side,  $I_{P(avg)}$ . This statement can be implicitly interpreted by equations of both  $V_{LM}$  and  $I_{P(avg)}$  being proportional to the peak value of the magnetizing inductor current  $I_{LM(peak)}$ , which is stated as (4) and (5).

$$V_{LM} \propto I_{P(avg)}$$
  $\left\{ \begin{array}{c} V_{LM} \propto I_{LM(peak)} & ... \\ I_{LM(peak)} \propto I_{P(avg)} & ... \end{array} \right.$  (4)

For a flyback converter, if the conduction period  $t_{on}$  and the magnetizing inductance  $L_M$  are fixed, equation (4) will stand for reason according to equation (6) regardless of operations in either DCM or BCM. Meanwhile, based on equation (7),  $D_{on}$  has to be kept constant, which in turns indicates the period of the switching cycle  $T_S$  must also be kept constant. Therefore, variations of  $L_M$ ,  $t_{on}$ ,  $D_{on}$ , and  $T_S$  must be small in order to obtain a high PF design.

$$V_{LM} = L_M \frac{I_{LM(peak)}}{t_{on}} \tag{6}$$

$$I_{P(avg)} = \frac{1}{2} \frac{I_{LM(peak)} t_{on}}{T_s} = \frac{1}{2} \frac{I_{LM(peak)} D_{on} T_s}{T_s} = \frac{1}{2} I_{LM(peak)} D_{on} \dots (7)$$

If the transformer is properly designed, the magnetizing inductance  $L_M$  should be constant without core saturation. By adjusting the system response to be slower than the input line frequency,  $t_{on}$  can be guaranteed relatively constant for several successive line cycles. Besides, an operation in DCM indicates a fixed-frequency operation, which means  $T_S$  and  $D_{on}$  will be constant and therefore a high power factor can be achieved. On the other hand, BCM is an inherent variable-frequency operation in nature; therefore  $T_S$  and  $D_{on}$  will not be constant and achievable power factor is relatively low. Users should be fully aware of the trade-off between operations in DCM and BCM.



## **Quasi-Resonant Function**

Fig.3 illustrates typical switching waveforms of a quasi-resonant flyback converter. When the magnetizing inductor is fully discharged, the residue charge on the MOSFET parasitic capacitance Cds induces a resonant between the magnetizing inductor  $L_M$  and  $C_{ds}$ . As illustrated in Condition 1, MBI6812 detects the first valley of the resonant response and turns on the MOSFET to initiate the very next switching cycle. In some applications, as depicted in Condition 2, the MOSFET is turned on at another relative valley of the resonant due to minimum switching period limitation (8.33 $\mu$ s, or equivalently 120kHz maximum switching frequency). In both cases, the switching loss is minimized and the radiation EMI is alleviated because to the onset of each switching cycle is at the voltage valley.

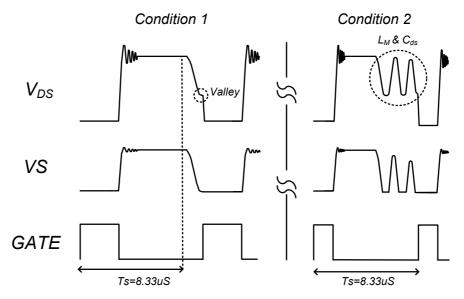


Fig.3 Typical quasi-resonant switching waveforms of MBI6812



## **Start-up Circuit**

A simplified equivalent circuit of MBI6812 during power-on period is illustrated in Fig.4. When power on, the  $V_{DD}$  slowly rises up in a time constant, which is set by  $R_{ST}$  and  $C_{DD}$ . Once the  $V_{DD}$  achieves the start up voltage,  $V_{DD-ON}$ , MBI6812 starts normal operation, and the current consumption increases from  $I_{DD\_ST}$  to  $I_{DD\_NORMAL}$ . Before the output voltage builds-up, the current consumption in steady state,  $I_{DD\ NORMAL}$  is supplied by  $C_{DD}$ . Figure 8 shows the waveforms of GATE between the start-up period and the steady state. MBI6812 built-in a speed up circuit to shorten the start-up period, the pulse width of GATE in start-up period would be four times greater than the steady state. In general, the converter with active power factor correction needs a large output capacitor to suppress the output current ripple; however, the large output capacitor is a trade off with the start-up period. The start-up period also can be shortened by small  $R_{ST}$ .

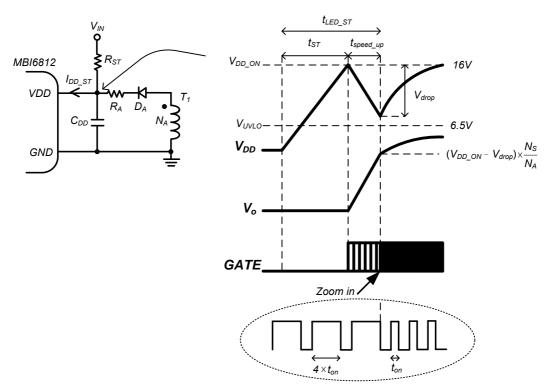


Fig.4 Equivalent circuit for start-up period and corresponding waveforms

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# **Over Voltage Protection**

The build-in over voltage protection is implemented by VDD pin. When the voltage on VDD exceeds 21V due to the abnormal voltage on auxiliary winding, the GATE signal will stop switching immediately and shut off MBI6812 until the  $V_{DD}$  voltage drops to UVLO.

## **LED Open-Circuit Protection**

The operation of LED open-circuit protection is illustrated in Fig.5. When LED is opened, the voltage on VS pin rises with the output voltage; once the  $V_S$  voltage achieves the threshold voltage of open circuit protection (1.5V), the GATE signal will stop switching until the  $V_{DD}$  voltage drops to UVLO. When the  $V_{DD}$  drops to UVLO, and then the converter will restart from soft start mode again. The cycle will be repeated until the fault is removed.

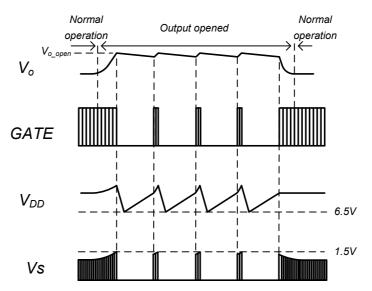


Fig.5 Conceptual waveform of  $V_O$ , GATE,  $V_{DD}$  and  $V_S$  when output is opened and recovered



# **LED Short-Circuit Protection**

The operation of LED short-circuit protection is illustrated in Fig.6. The LED short circuit is detected when the  $V_S$  drops to zero and  $V_{CS}$  exceeds 0.6V. Once the LED short-circuit failure occurs, the *GATE* signal will stop switching and shut off MBI6812 until the  $V_{DD}$  drops to UVLO, and then the converter will restart from soft start mode again. The cycle will be repeated until the fault is removed.

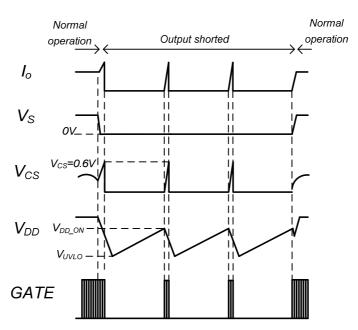


Fig.6 Conceptual waveforms of Io, Vs, Vcs, VDD, and GATE when output is shorted and recovered

### **Current Sense Resistor Failure Protection**

To prevent the MOSFET being burned out due to the CS pin short to GND, which caused by the solder error, MBI6812 provides the current sense resistor failure protection. When the voltage on CS pin drops to zero, the GATE turns off immediately and then  $V_{DD}$  drops to UVLO. When  $V_{DD}$  achieves UVLO, the  $C_{DD}$  recharged to the enable voltage (16V) and IC starts again. The protection will keep activating until the failure been removed.

## **Compensation Capacitor Failure Protection**

To prevent the circuit being burned out due to the *COMP* pin floating, which caused by the solder error, MBI6812 provides the *COMP* pin floating protection. When the COMP pin is floating, the *GATE* turns off immediately and then  $V_{DD}$  drops to UVLO. When  $V_{DD}$  achieves UVLO, the  $C_{DD}$  recharged to the enable voltage (16V) and IC starts again. The protection will keep activating until the failure been removed.



## **Design Procedure**

# Step 1. Input Power, $P_{\text{IN}}$ , and Output Power, $P_{\text{O}}$

Output power  $P_o$  and input power  $P_{in}$  can be calculated by

$$P_{o} = V_{o} \times I_{o} \tag{8}$$

$$= \eta \times P_{IN} = 0.83 \times P_{IN} \tag{9}$$

where  $\eta$  is the conversion efficiency, and it is estimated to be approximately 83%.

### Step2. Magnetizing Inductance, $L_M$

Assume the power factor is 1, then the  $P_{IN}$  can be calculated by

$$P_{lN} = V_{rms} \times I_{rms} \tag{10}$$

$$=\frac{V_{AC,peak}}{\sqrt{2}}\times\frac{I_{AC,peak}}{\sqrt{2}}$$
 (11)

#### where

 $V_{AC,peak}$  is the peak voltage of AC input source.

 $I_{AC,peak}$  is the peak current of AC input source.

When the switching frequency  $f_S$  is much larger than the AC frequency, the relationship between  $I_{AC,peak}$  and  $I_{p,peak}$  can be equivalent to the following formula.

$$I_{AC,peak} = \frac{1}{T_s} \int_0^{D_{on}T_s} \frac{I_{p,peak}}{D_{on}T_s} t dt \qquad (12)$$

$$=\frac{D_{on}}{2}\times I_{p,peak}$$
 (13)

#### where

 $I_{p,peak}$  is the peak current of primary side of the transformer.

 $D_{on}$  is the duty ratio of  $S_1$ .

 $T_{\rm S}$  is the switching period.

When the converter operates in DCM and BCM,  $I_{p,peak}$  can be calculated by

$$I_{p,peak} = \frac{V_{AC,peak} \times D_{on}}{L_{u} \times f_{c}} \tag{14}$$

Combine (11), (13), and (14)

$$L_{M} = \frac{(V_{AC,peak} \times D_{on})^{2}}{4 \times P_{IN} \times f_{S}}$$
 (15)



For the EMI consideration, the mixed mode of BCM and DCM is recommended. Suppose  $V_{AC,max}$  is 265V,  $V_{AC,min}$  is 85V, the operation is shown in Figure 7. The  $f_{S,SL,ACmin}$  is the slowest switching frequency, it will happen on the peak of  $V_{AC,min}$ . The  $f_{S,Fa}$  is fastest switching frequency, it will happen in DCM, and the default is 120kHz.

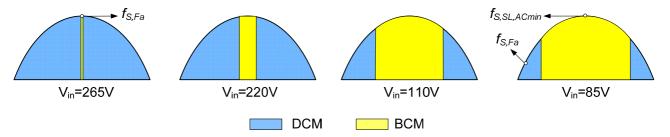


Fig.7 The suggested distribution of DCM and BCM

When design the transformer, the maximum peak current of primary side,  $I_{p,peak,max}$ , mush be calculated first. The  $I_{p,peak,max}$  happens at the minimum input voltage,  $V_{AC,min,peak}$ , and it also leads the slowest switching frequency,  $f_{S,SL,ACmin}$ , and the maximum duty ratio,  $D_{on,max}$ . Thus, (15) can be expressed as

$$L_{M} = \frac{(V_{AC,min,peak} \times D_{on,max})^{2}}{4 \times P_{IN} \times f_{S,S,I,AC,min}}$$
(16)

The recommended  $D_{on,max}$  is 0.3~0.45, and designed at 0.45 can obtain better efficiency. If the desired operation mode is similar to Fig.11, the  $V_{AC,max}$ ,  $V_{AC,min}$ , and  $f_{S,Fa}$  must be determined first, and then  $f_{S,SL,ACmin}$  can be calculated by

$$f_{S,SL,AC\,min} = f_{S,Fa} \times [(\frac{V_{AC,min}}{V_{AC,max}} - 1) \times D_{on,max} + 1]^2$$
 (17)

 $I_{p,peak,max}$  can be calculated by substituting the  $V_{AC,min,peak}$ ,  $f_{S,SL,ACmin}$ ,  $D_{on,max}$ , and  $L_M$  into (14).

#### Step 3. Turn ratio, $N_P : N_S : N_A$

After deciding  $D_{on,max}$ , the  $D_{dsc}$  can be calculated by follows

$$\frac{V_o + V_{F\_Do}}{V_{AC\ min\ peak}} = \frac{N_S \times D_{on,max}}{N_P \times D_{dsc}} \tag{18}$$

where

 $V_{F\ Do}$  is the forward voltage of output diode Do.

 $D_{dsc}$  is the discharging time ratio of magnetizing inductance  $L_{M}$ .

The condition for the flyback converter in BCM is

$$D_{on,max} + D_{dsc} = 1 (19)$$

Combine (18) and (19)

$$\frac{N_P}{N_S} \le \frac{V_{AC,min,peak} \times D_{on,max}}{(V_o + V_{F_Do}) \times (1 - D_{on,max})}$$
(20)

If the transformer winding space is enough, the turn ratio should be equal to (20). If the space is not allowed, the smaller turn ratio results the more BCM distribution and slower  $f_{S,SL,ACmin}$ , also the transformer may be



saturated. Oppositely, the larger turn ratio results the less BCM distribution but higher TVS voltage, which might cause overheat problem. (21) can be used when choosing the TVS,

$$V_{TVS,VRWM} > \frac{N_P}{N_S} \times (V_O + V_{F_DO})$$
0.8 (21)

where  $V_{TVS,VRWM}$  is the reverse stand-off voltage of TVS.

(22) is to determine the turn number of primary side. Consider 10% tolerance to the actual inductance, the actual turn number should be 1.05 times larger than the calculated

$$N_{P} \ge \frac{1.05 \times L_{M} \times I_{p,peak,max}}{B_{max} \times A_{e}}$$
 (22)

where  $B_{max}$  is the maximum magnetic flux density of core and  $A_e$  is the core effective area. These two parameters can be found from the core datasheet.

The recommended normal operating voltage,  $V_{DD\_normal}$ , is 12V~16V, should be determined before designing the turn ratio  $N_S/N_A$ . Because the loading of the secondary side is higher than that of the auxiliary side, the relationship of secondary and auxiliary voltage is estimated as

$$\frac{N_{S}}{N_{A}} = \frac{V_{o} + V_{F\_Do}}{0.95 \times (V_{DD\_normal} + V_{F\_DA})}$$
(23)

The actual turn number of each winding should be an integer. After  $N_P$ ,  $N_S$ , and  $N_A$  have been determined,  $D_{dsc,rms}$  can be obtained from (24).

$$D_{dsc,rms} = \sqrt{\frac{2 \times I_o \times L_m \times f_{S,SL,ACmin}}{(V_o + V_{F,Do})}} \times \frac{N_S}{N_P}$$
(24)

#### Step 4. MOSFET, S<sub>1</sub>

The maximum drain-source breakdown voltage of S1 can be calculated by

$$V_{DS1,max} \ge \frac{(\sqrt{2} \times V_{ac,max} - V_{F\_DBR} + V_{TVS})}{0.8}$$
 (25)

where

 $V_{DS1,max}$  is the maximum drain-source breakdown voltage of  $S_1$ .

 $V_{F\ DBR}$  is the forward voltage of bridge rectifier  $D_{BR}$ .

 $V_{TVS}$  is the breakdown voltage of TVS.

The maximum drain-source breakdown voltage of  $S_1$  will vary with the breakdown voltage of TVS. The lower breakdown voltage of TVS also results the lower efficiency, and vice versa. Consider the availability of efficiency and the component, a MOSFET with 600V maximum drain-source breakdown voltage is recommended for  $S_1$ . Substituting the determined  $V_{DS1,max}$  into (25),  $V_{TVS}$  can be obtained.

The maximum current of  $S_1$  can be expressed as



$$I_{S1,max} \ge \frac{I_{p,peak,max}}{0.8}$$
 (26)

The MOSFET with higher rated current features the lower equivalent conduction resistance ( $R_{ds(on)}$ ) and therefore conduction loss. However, it also features higher equivalent capacitance ( $C_{iss}$  and  $C_{oss}$ ) and therefore switching loss. Thus, the recommended rated current of MOSFET should be large but close to (26).

### Step 5. Transient Voltage Suppressor, TVS

After Step 4, please use (21) to reconfirm the breakdown voltage of TVS. If they are conflicted, please increase the maximum drain-source breakdown voltage of S1 or reduce the  $D_{on,max}$  and  $N_P/N_S$ . Besides, the peak power dissipation of TVS is suggested to be higher than 600W.

### Step 6. Current Sensing Resistor, R<sub>CS1</sub>

 $V_{cs,pk,rms}$  can be expressed as

$$V_{cs,pk,rms} = \frac{I_{p,peak,max} \times R_{cs1}}{\sqrt{2}}$$
 (27)

The product of  $V_{cs,pk,rms}$  and  $D_{dsc,rms}$  in MBI6812 is defaulted to 0.1V.

$$V_{cs,pk,rms} \times D_{dsc,rms} = 0.1 \dots (28)$$

Combine (28) and (29):

$$R_{cs1} = \frac{0.1 \times \sqrt{2}}{D_{dsc,rms} \times I_{p,peak,max}}$$
 (29)

Substituting  $D_{dsc,rms}$  and  $I_{p,peak,max}$  into (29),  $R_{cs1}$  can be calculated. However, the calculated resistance might not correspond with the actual value, thus, the connection ( $R_{CS1} \sim R_{CS3}$ ) shown in Fig. 8 is recommended. The resistance of  $R_{CS1}$  is approximately 0.1~1 $\Omega$ . Consider the effects of noise rejection and loading effect, the resistances of  $R_{CS2}$  and  $R_{CS3}$  are suggested to be in the range of 1k~30k $\Omega$ . In addition, the package type of  $R_{CS1}$  should be 1206, and  $R_{CS2}$  and  $R_{CS3}$  should be 0603.

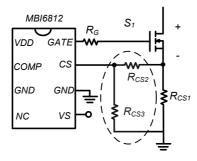


Fig.8 Application circuit of  $R_{CS2}$  and  $R_{CS3}$ 



## Step 7. Bridge Rectifier, $D_{BR}$

The maximum reverse voltage and forward current of the bridge rectifier  $D_{BR}$  is suggested to satisfy the following conditions

$$V_{DBR,max} \ge \frac{\sqrt{2} \times V_{ac,max}}{0.8}$$
 (30)

$$I_{DBR,max} \ge \frac{\sqrt{2} \times P_{in}}{0.8 \times V_{ac.min}}$$
 (31)

## Step8. Output Diode, Do

The maximum reverse voltage and forward current of the output diode  $D_o$  should satisfy the following conditions

$$V_{Do,max} \ge \frac{\frac{N_s}{N_p} \times \sqrt{2} \times V_{ac,max} + V_o}{0.8}$$
 (32)

$$I_{Do,max} \ge \frac{\frac{N_P}{N_S} \times I_{p,peak,max}}{0.8} \tag{33}$$

The super-fast or ultra-fast diode with short reverse recovery time ( $t_{rr}$  < 50ns) and low forward voltage ( $V_F$ ) is recommended. If the measured temperature of  $D_o$  is too high, it is suggested to choose the diodes with higher rated current, lower forward voltage, and larger package.

#### Step 9. Output Capacitor, Co

The recommended rated voltage of  $C_o$  is 1.2 times higher than the output over voltage protection level. The higher capacitance of the output capacitor can reduce the output current ripple; also, the efficiency will be raised. However, the higher capacitance of the output capacitor needs larger volume, and longer start-up time. When select electrolytic capacitor, the sustainable ripple current (RMS) should be larger than (34)

$$I_{Co,Rated,ripple} > \frac{\sqrt{(I_{s,peak,max})^2 \times \frac{(1-D_{on,max})}{3} - (I_o)^2}}{0.8}$$
 (34)

## Step 10. Auxiliary Diode, $D_A$

The maximum reverse voltage of the auxiliary diode  $D_A$  should satisfy the following equation

$$V_{DA,max} \ge \frac{\frac{N_A}{N_P} \times \sqrt{2} \times V_{ac,max} + V_{DD}}{0.8}$$
 (35)

The diode which has short reverse recovery time ( $t_{rr}$  < 150ns) and high peak forward surge current



 $(I_{FSM} > 20A)$  is recommended. In addition, cascade a current limit resistor RA ( $= 20\Omega$ ) to  $D_A$  for suppressing the voltage spike on the auxiliary winding and regulating supply voltage  $V_{DD}$  is recommended.

### Step 11. Snubber Diode, Dsb

The maximum reverse voltage of the snubber diode  $D_{sb}$  should satisfy the following equation

$$V_{Dsb,max} \ge \frac{\sqrt{2} \times V_{ac,max} + V_{TVS}}{0.8}$$
 (36)

The diode which has short reverse recovery time ( $t_{rr}$  < 150ns) and high peak forward surge current ( $I_{FSM}$  > 20A ) is recommended.

### Step 12. Start-up Resistor, $R_{ST}$ , and Supply Capacitor, $C_{DD}$

When the system starts up,  $V_{DD}$  slowly rises in accordance with a time constant set by  $R_{ST}$  and  $C_{DD}$ . The start-up time  $t_{ST}$  can be expressed as

$$V_{DD} = V_{IN} \times (1 - e^{\frac{-t_{ST}}{R_{ST} \times C_{DD}}}) \qquad (37)$$

During the start-up time, the standby current of MBI6812 is  $I_{DD\_ST}$ , so the above equation can be modified as

$$V_{DD\_ON} = (V_{IN} - I_{DD\_ST} \times R_{ST}) \times (1 - e^{\frac{-t_{ST}}{R_{ST} \times C_{DD}}}) \qquad (38)$$

$$t_{ST} = -R_{ST} \times C_{DD} \times ln(1 - \frac{V_{DD\_ON}}{V_{IN} - I_{DD\_ST} \times R_{ST}})$$
 (39)

In the duration of start-up period, once the  $V_{DD}$  exceeds  $V_{DD\_ON}$ , MBI6812 into speed-up mode, and the current consumption is supplied by  $C_{DD}$ , the relationship can be expressed as

$$V_{drop} = \frac{1}{C_{DD}} \int I_{DD\_normal} \cdot dt \qquad (40)$$

where  $V_{drop}$  means the UVLO of MBI6812, then the (40) can be modified as

$$t_{\text{speed\_up}} = \frac{V_{\text{drop}} \times C_{\text{DD}}}{I_{\text{DD}} \text{ NORMAL}}$$
 (41)

In MBI6812,  $V_{DD\_ON}$ =16V,  $V_{UVLO}$  =8V,  $I_{DD\_NORMAL}$  =3.5mA, and  $I_{DD\_ST}$  =10uA.  $t_{ST}$  can be calculated by (40), and  $t_{speed\_up}$  can be calculated by (41). In this example, the start-up and speed-up periods are 550ms and 10.7ms respectively by  $R_{ST}$ =1M $\Omega$  and  $C_{DD}$ =4.7uF. If the sum of start-up time and speed-up time is larger 1s, which is the popular requirement in LED lighting application, decrease the resistance of  $R_{ST}$  is helpful to speed up the period, but side effect is the decreased efficiency. Due to the  $R_{ST}$  must sustain higher voltage stress when applied in universal voltage application, two halves resistors with 1206 package in cascaded is recommended.



## Step 13. Voltage Sensing Resistor, $R_{VS1}$ and $R_{VS2}$

MBI6812 detects the LED open-circuit through  $V_S$  pin, and the threshold voltage of LED open-circuit protection is set by  $R_{VS1}$  and  $R_{VS2}$ . The recommended resistance of  $R_{VS2}$  is  $30\text{k}\Omega$ , and  $R_{VS1}$  can be calculated from

$$R_{VS1} = \left(\frac{1.2}{(V_{DD\_Normal} + V_{F\_DA}) \times R_{VS2}}\right)^{-1} - R_{VS2}$$
 (42)

By the above formula design, the voltage of LED open-circuit protection is 1.25 times larger than the voltage of LED. If the actual threshold voltage of LED open-circuit protection is larger than the expected, user can decrease the  $R_{VS1}$ , and vice versa.

In addition, the resistances of  $R_{VS1}$  and  $R_{VS2}$  also relate to the line compensation, if the output current increases with the increased input voltage, user can reduce the resistances of  $R_{VS1}$  and  $R_{VS2}$  but keep the same ratio, and vice versa.

### Step 14. Compensation Resistor, C<sub>COMP</sub>

 $C_{COMP}$  can be used to control the converter response. The larger capacitance brings the slower response, higher PF, and also the slower start-up time. Therefore, the capacitance can be adjusted depends on the actual application. The recommended capacitance is ranging from 1uF and 4.7uF.

#### Step 15.Input Capacitor, C<sub>IN</sub>

In order to enhance the PF, the capacitance of  $C_{IN}$  smaller than 50nF is recommended.  $C_{IN}$  should be placed as close as possible to the  $S_1$  and transformer.



## **Estimated Efficiency**

To estimate the efficiency, the power consumption on each current carrying component must be calculated and summed up. The efficiency  $(\eta)$  can be described as

$$\eta = P_o / (P_o + P_{Loss}) \times 100\%$$

The total power loss ( $P_{LOSS}$ ) in flyback converter based on MBI6812 includes

$$P_{LOSS} = P_{BR} + P_{RST} + P_{RCS} + P_{S1\_C} + P_{S1\_SW} + P_{Do} + P_{Ro} + P_{TVS} + P_{Np\_C} + P_{Ns\_C} + P_{IC}$$

 $P_{BR}$  is the power loss on  $D_{BR}$ ,  $P_{BR} = V_{BR\_F} \times I_{p,peak,max} \times D_{on,max} \times 2/3.14$ ,  $V_{BR\_F}$  is the forward voltage of  $D_{BR}$ .  $P_{RST}$  is the power dissipation of  $R_{ST}$ ,  $P_{RST} = [(V_{AC,min,peak} - V_{DD})/\sqrt{2}]^2/R_{ST}$ .

 $P_{RCS1}$  is the power dissipation of  $R_{CS1}$ ,  $P_{RCS1} = (I_{p,peak,max} \times D_{on,max} \times 1/3.14)^2 \times R_{CS1}$ .

 $P_{S_{1}C}$  is the conduction loss of the power MOSFET  $S_{1}$ ,  $P_{S_{1}C} = (I_{p,peak,max} \times D_{on,max} \times 1/3.14)^{2} \times R_{DS(on)}$ ,  $R_{DS(on)}$  is the equivalent on-resistance of  $S_{1}$ .

 $P_{S1\_SW}$  is the switching loss of the power MOSFET  $S_1$ ,  $P_{S1\_SW} = [V_{AC,min} + (N_P/N_S) \times (V_o + V_{Do\_F})] \times (I_{p,peak,max} / \sqrt{2}) \times t_f \times f_{S,Fa} / 2$ .  $t_f$  is the falling time of the switching signal, and it can be estimated as  $t_f = 60$ ns  $\times C_{GS} / 1$ nF; where  $C_{GS}$  is the gate-to-source capacitance of MOSFET, which can be found in datasheet.

 $P_{Do}$  is the power dissipation of  $D_o$ ,  $P_{Do} = V_{F_Do} \times I_o$ .

 $P_{Ro}$  is the power dissipation of  $R_{Ro}$ ,  $P_{Ro} = V_o^2 / R_{o1}$ .

 $P_{TVS}$  is the switching loss of TVS,  $P_{TVS} = 1/4x L_k \times I_{p,peak,max}^2 \times f_{S,Fa}$ ,  $L_k$  is the leakage inductance of transformer T1 and it can be measured by LCR meter.

 $P_{Np\_C}$  is the copper loss of the primary side of transformer  $T_1$ ,  $P_{Np\_C} = (I_{p,peak,max} \times D_{on,max} \times 1/3.14)^2 \times R_{Np}$ ,  $R_{Np}$  is the DC resistance (DCR) of the primary side of transformer T1 and it can be measured by LCR meter.

 $P_{Ns\_C}$  is the copper loss of the secondary side of transformer  $T_1$ ,  $P_{Ns\_C} = ((N_P/N_S)x I_{p,peak,max} x (1-D_{on,max})x 1/3.14)^2x R_{Ns}$ ,  $R_{NS}$  is the DC resistance (DCR) of the secondary side of transformer T1 and it can be measured by LCR meter.

 $P_{IC}$  is the power consumption of MBI6812,  $P_{IC} = V_{DD} \times I_{DD}$ .



## **Design Example**

_	
System Requirements for Driving 26W LED Lamp	
Input Voltage	85~265 V <sub>AC</sub> /60Hz
Output Current	500mA
Output Voltage	52V
VDD Normal Operating Voltage	16V
Maximum Duty Ratio, Don,max	0.45
Fastest Switching Frequency, $f_{S,Fa}$	120kHz
Core Parameter (3C90 RM-8)	
Saturation magnetic flux density (100°C), B <sub>max</sub>	0.32T
Effective area, A <sub>e</sub>	64.9mm <sup>2</sup>

- 1. From (8) and (9), Po=26W, Pin=31.32W.
- 2. From (17),  $f_{S,SL,ACmin}$ =57.85kHz.
- 3. From (16) and (14),  $L_M$  = 390uH,  $I_{p,peak,max}$  = 2.39A  $\circ$
- 4. From (26), the maximum current of S1 is  $I_{S1} \ge 3A$ . For universal input applications, MOSFET with 650V maximum drain-source breakdown voltage is the most popular choice. The recommended selection of S1 with 650V maximum drain-source breakdown voltage and 7A maximum drain current. Its gate-source capacitance  $C_{GS}$ =990pF.
- 5. From (25), the breakdown voltage of TVS is  $V_{TVS}$ =147.23V. The recommended selection of TVS is P6SMJ120A ( $V_{TVS,VRWM}$ =120V)manufactured by PANJIT with 133~169V breakdown voltage and 600W peak pulse power dissipation.
- 6. From (20), the turn ratio is  $N_P/N_S \le 1.83$ . Substitute  $N_P/N_S = 1.5$  into (21), then the calculated result meets the above requirement. The  $D_{dsc,rms}$  can be calculated by (24),  $D_{dsc,rms} = 0.45$ .
- 7. From (23),  $N_S / N_A = 3.29$ . And then from (22),  $N_P=47$  turns,  $N_S=32$  turns,  $N_A=10$  turns.
- 8. From (29),  $R_{cs1} = 1.3\Omega$ . Choose  $R_{CS1} = 1.4\Omega$ ,  $R_{CS2} = 1k\Omega$ ,  $R_{CS3} = 9.1K\Omega$ .
- 9. From (30) and (31),  $V_{DBR,max} \ge 465.9 \text{V}$  and  $I_{DBR,max} \ge 0.7 \text{A}$  respectively. The recommended selection of DBR is TB8S manufactured by PANJIT with 800V reverse voltage and 1A maximum average forward current.
- 10. From (32) and (33),  $V_{Do,max} \ge 375.64 \text{V}$  and  $I_{Do,max} \ge 4.49 \text{A}$  respectively. The recommended selection of



D<sub>O</sub> is ER504 manufactured by PANJIT with 400V reverse voltage and 5A maximum average current.

- 11. 270uF/100V electrolytic capacitor is used for C<sub>O</sub> because space issue is very important in E27 LED lamp applications. In addition, it uses two capacitor with parallel for consistent with (34).
- 12. From (35),  $V_{DA,max} \ge 114.47$ V. The recommended selection of  $D_A$  is ES1002 manufactured by PANJIT with 200V reverse voltage and 30A peak forward surge current.
- 13. From (36),  $V_{DSB,max} \ge 600 \text{V} \cdot \text{The recommended selection of } D_{SB}$  is ES1006 manufactured by PANJIT with 600V reverse voltage and 30A peak forward surge current.
- 14. Choose  $R_{ST}$ =1M $\Omega$  and  $C_{DD}$ =4.7uF. The start-up time is about 0.75s.
- 15. From (42),  $R_{VS1}$ =390k $\Omega$ ,  $R_{VS2}$ =30k $\Omega$ .

## **Estimated Efficiency**

The power consumption on each component at VAC=85V can be calculated by

$$P_{BR} = V_{BR\_F} \times I_{p,peak,max} \times D_{on,max} \times 2/3.14 = 2V \times 2.39A \times 0.45 \times 2/3.14 = 1373 \text{mW}$$

$$P_{RST} = [(V_{AC,min,peak} - V_{DD})/\sqrt{2}]^2/R_{ST} = [(120.2V - 16V)/\sqrt{2}]^2/1M\Omega = 5.12 \text{ mW}$$

$$P_{RCS1} = = (I_{p,peak,max} \times D_{on,max} \times 1/3.14)^2 \times R_{CS1} = (2.39 \text{A} \times 0.45 \times 1/3.14)^2 \times 0.15 \Omega = 17.68 \text{mW}$$

$$P_{S1\_C} = (I_{p,peak,max} \times D_{on,max} \times 1/3.14)^2 \times R_{DS(on)} = (2.39 \text{A} \times 0.45 \times 1/3.14)^2 \times 1.4\Omega = 164.99 \text{ mW}$$

$$P_{S1\_SW} = [V_{AC,min} + (N_P/N_S) \times (V_o + V_{Do\_F})] \times (I_{p,peak,max} / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times t_f \times f_{S,Fa} / 2 = [85V + (1.5) \times (52.95V)] \times (2.39A / \sqrt{2}) \times (2.39A /$$

59.4ns x 120kHz/2 = 992.6 mW

$$(t_f = 60 \text{ns } \times 990 \text{pF} / 1 \text{nF} = 19.8 \text{ns})$$

$$P_{Do} = V_{FDo} \times I_{o} = 0.95 \text{V} \times 0.5 \text{A} = 475 \text{mW}$$

$$P_{Ro1} = V_o^2 / R_{o1} = (52 \text{V x } 52 \text{V}) / 51 \text{k}\Omega = 53.02 \text{mW}$$

$$P_{TVS} = 1/4 \text{x } L_k \text{ x } I_{p,peak,max}^2 \text{x } f_{S,Fa} = 1/4 \text{ x} 3.9 \text{uH x } (2.39 \text{A})^2 \text{x } 120 \text{ kHz} = 671.35 \text{ mW}$$

(Measured  $L_k = 3.9 \text{uH}$ )

$$P_{Np,C} = (I_{p,peak,max} \times D_{on,max} \times 1/3.14)^2 \times R_{Np} = (2.39 \text{A} \times 0.45 \times 1/3.14)^2 \times 2\Omega = 235.7 \text{ mW}$$

(Measured  $R_{Np} = 2\Omega$ )

$$P_{Ns\_C} = ((N_P/N_S)x \ I_{p,peak,max} \ x \ (1-D_{on,max})x \ 1 \ /3.14)^2 x \ R_{Ns} = ((1.5)x \ 2.39A \ x \ (1-0.45)x \ 1 \ /3.14)^2 x \ 1 = 396.11 \ mW$$
 (Measured  $R_{Ns} = 1\Omega$ )

$$P_{IC} = V_{DD} \times I_{DD} = 16 \text{ V } \times 3.5 \text{mA} = 56 \text{ mW}$$

$$P_{LOSS} = P_{BR} + P_{RST} + P_{RCS} + P_{S1} + P_{S1} + P_{D0} + P_{R01} + P_{TVS} + P_{Np} + P_{Ns} + P_{N$$

Thus, the estimated efficiency of this application is

$$\eta = P_o / (P_o + P_{Loss}) \times 100\% = 26 / (26 + 4.44) \times 100\% = 85.41 \%$$



# **PCB Layout Guideline**

Refer to Fig.1, some PCB layout guidelines are explained below.

- 1. High current paths should be as wide and short as possible to eliminate parasitic effects.
- 2. Keeping a complete "GND" plane and placing the solder as wide as possible are helpful to alleviate the switching noise.
- 3. To avoid the parasitic effect, the pins of all components should be placed as short as possible.
- 4.  $R_{CS1}$ ,  $R_{CS2}$ , and  $R_{CS3}$  must be placed as close to CS pin as possible.
- 5.  $R_{VS1}$ , and  $R_{VS2}$  must be placed as close to VS pin as possible.
- 6.  $C_{CF}$  must be placed as close to COMP pin as possible.
- 7.  $C_{IN}$  and  $S_1$  must be placed as close as possible to the primary side of the transformer T1 to minimize the switching current loop which is shown as the blue line in Fig.9 and Fig.10.
- 8. *Do* and *Co* must be placed as close as possible to the secondary side of the transformer *T1* to minimize the switching current loop which is shown as the green line in Fig.9 and Fig.10.
- 9. In order to avoid IC be influenced by noise, please separate *COMP* away from MOSFET, transformer, and the circuit of high voltage spike.
- 10.Please increase the copper pour area of IC's ground plane. If the PCB size is limited, please follow the sketch of fig.11 to connect the different types of ground plane. GND1 and GND2 are ground with switching circuit, GND3 is the signal ground. Please gathering GND1~GND3 separately, and then connect to the negative terminal of *C*<sub>IN</sub> capacitor.

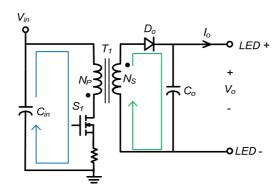


Fig.9 Blue and green lines shows the current loops of S1 on and off period respectively.

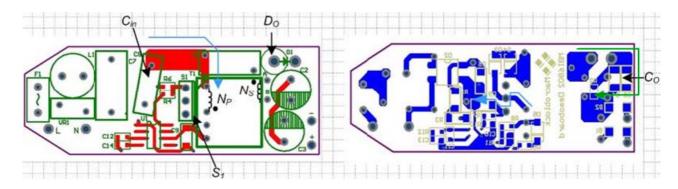


Fig.10 Layout example



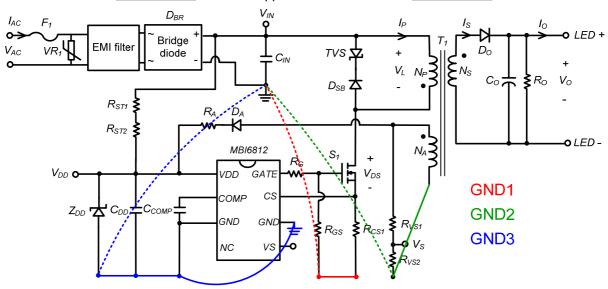


Fig.11 Recommended ground layout

## **Transformer winding Guideline**

- The recommended winding order of the transformer is shown as Fig.12, Primary(N1)→Auxiliary(N2)→Secondary(N3)→Primary(N4).
- 2. The recommended starting point of transformer windings is from the drain terminal of MOSFET.

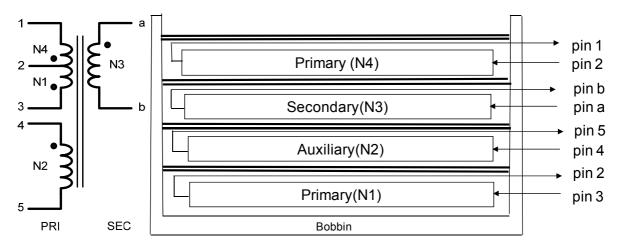


Fig.12 Transformer structure